EGC221: Digital Logic Lab

Experiment #5

Arithmetic Circuits Using Altera Quartus Prime

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Assessment:

Assessment Point	**Weight**	**Grade**
Methodology and correctness of results		
Discussion of results		
Participation		
Assessment Points' Grade:		

Comments:

Experiment #5:

Full Adder Circuit Implementation

Objectives:

The objectives of this experiment are to:

1. Get familiar with Altera Quartus Pime
2. implement a full-adder using logic gates,
3. implement a 4-bit ripple carry adder (using logic gates), and
4. Modify the 4-bit adder such that it is capable of 4-bit addition/subtraction.

Procedure:

1. Become familiar with Altera Quartus Prime toolset by going through the Tutorial on Quartus Prime Schematic Capture.
2. Use Altera's Quartus Prime Schematic to solve Exercise 1.

Exercise 1:

(a) Given Table 1 below, complete the truth table for a full adder, and derive the logic expression for Sum and Cout.

Table 1. 1-bit Full Adder using basic gates truth table

A	B	Cin	**Sum**	**Cout**
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Logic Expression:	Sum:
Logic Expression:	Cout:

(b) Use Quartus Prime Schematic to provide the full-adder circuit diagram:

[Insert circuit diagram here]

Figure 1. Quartus Prime circuit diagram of full-adder

(c) Use Quartus Prime Schematic to provide functional and timing verifications:

[Insert functional verification timing diagram here]

[Insert timing verification timing diagram here]

Figure 2. Quartus Prime simulations of full adder
(functional is shown on top, and timing below)

Next, create a block diagram of the design in Figure 1 per Quartus Prime Schematic tutorial and continue with Exercise 2.

Exercise 2:

Using the circuit design from exercise 1 (Full Adder) and a hierarchical approach (as shown in Figure 3 below), create a 4-bit Binary Ripple Adder.

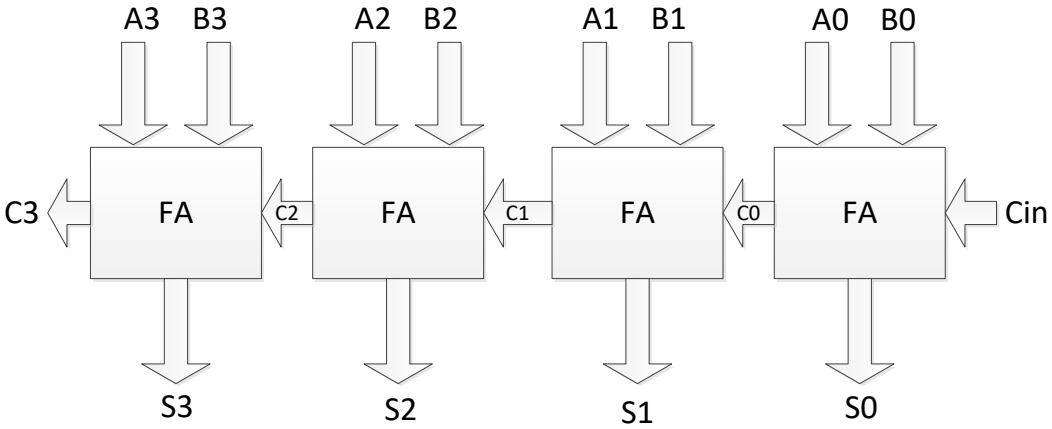

Figure 3. Hierarchical block diagram of 4-bit adder

(d) Use Quartus Prime Schematic to provide the 4-bit adder diagram:

[Insert circuit diagram here]

Figure 4. Quartus Prime circuit diagram of 4-bit adder

(e) Use Quartus Prime Schematic to provide functional and timing verifications:

[Insert functional verification timing diagram here]

[Insert timing verification timing diagram here]

Figure 5. Quartus Prime simulations of 4-bit adder
(functional is shown on top, and timing below)

Exercise 3:

Modify the 4-bit adder from part (d), to implement a 4-bit adder/subtractor.

(f) Use Quartus Prime Schematic to provide the 4-bit adder/subtractor circuit diagram:

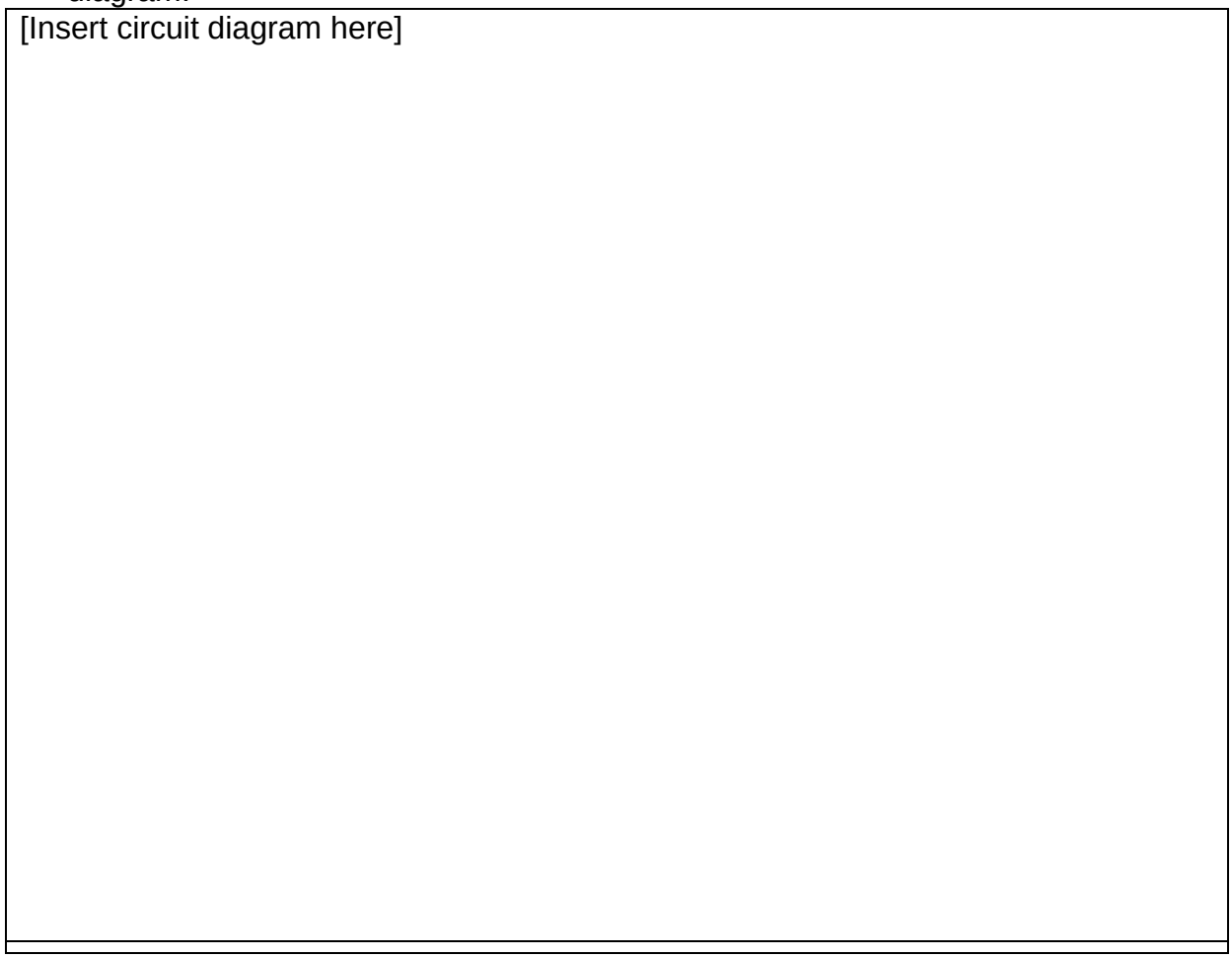

Figure 6. Quartus Prime circuit diagram of 4-bit adder/subtractor

(g) Use Quartus Prime Schematic to provide functional and timing verifications:

[Insert functional verification timing diagram here]

[Insert timing verification timing diagram here]

Figure 7. Quartus Prime simulations of 4-bit adder/subtractor circuit (functional is shown on top, and timing below)

Finally, verify the circuit by downloading on Altera DE10 board and have it signed by your instructor or TA.

Conclusions: